System and Method for Probabilistic Criticality

Prediction of Digital Circuits

5   ABSTRACT

The present invention is a system and method for determining criticality probability of

each node, edge and path of the timing graph of a digital circuit in the presence of delay

variations. The delay of each gate or wire is assumed to consist of a nominal portion, a

10   correlated random portion that is parameterized by each of the sources of variation and an

independent random portion. Correlations are taken into account. Both early mode and

late mode timing are included; both combinational and sequential circuits are handled;

static CMOS as well as dynamic logic families are accommodated. The criticality

determination complexity is linear in the size of the graph and the number of sources of

15   variation. The invention includes a method for efficiently enumerating the critical path(s)

that is/are most likely to be critical.